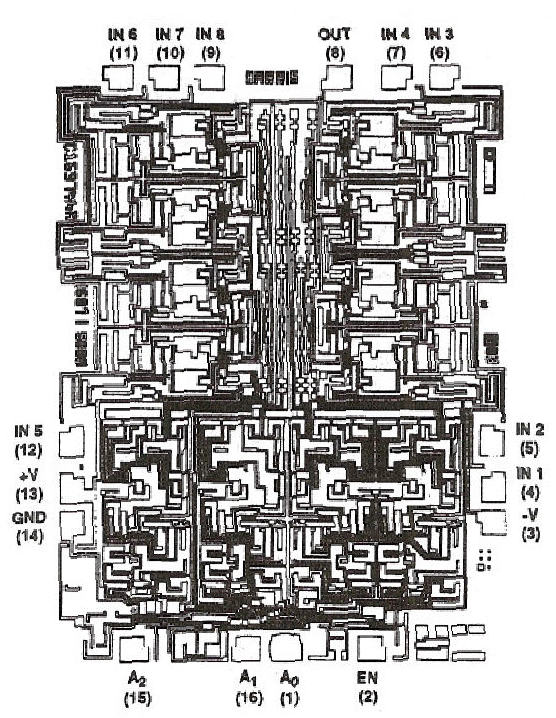
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” min.**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .083” X .108” DATE: 8/25/21**

**MFG: HARRIS THICKNESS .020” P/N: HI0-508**

**DG 10.1.2**

#### Rev B, 7/19/02